Logic:

Ghost Fin

First thing I would do is to get as much information about the yield issue as possible:

* Does it affect Sail yield at different voltage corners?
  + No, voltage independent
* Is it the entire lot? Or just a few wafers?
  + Most wafers in the lot to varying degrees
* Does it affect both Sail 1 and Sail 2 in the same way?
  + Affects different chips on Sail 1 and Sail 2. Sail 2 fails partial chips top, and full chips bottom, opposite for Sail 1.
* Is there any wafer regionality to the fails?
  + Top and bottom extreme edge.
* Is there any slot level dependency?
  + No
* Are there any splits on the lot?
  + No
* What blocks are failing most often? Is there a pattern to them?
  + 6,7,22,24,25
* What latches are on the blocks that are failing? Are they related?
  + X8M and X3M latches are the only ones failing
* Where are the blocks located in logic structure?
  + Not important
* What scan outs are failing more often on the block? Is it a specific scan chain that always fails?
  + Only specific scan outs failed. Looking closer at these scan outs we noticed that the fails only occur where there is a 2 Fin with 4 Fin RX below it
* Do the block fails have regionality dependence?
  + Yes
* Do the block fails have voltage dependence?
  + No
* Does it look like a systematic or random defect?
  + Wafer mishandling? One time thing?
  + Wafer misprocessing? Tool issue?
  + How will it correlate to the product die?

Next I would look for correlations, do data mining, consult experts, while having regular updates to the rest of the team

* The we consulted experts and requested an SEM to see that there is a short between the gate and a metal contact due to an incomplete etch. Somehow the 4fin RX structure caused an incomplete etch leading to this short.

If it seems to be a recurring problem I would set up a form of monitoring the defect, write a classification algorithm to automatically label this issue and also come up with some sort of metric to label how much of an impact to yield this specific defect has.

* It wasn’t an easy fix issue because it was related to how the latch was designed. Therefore I created the Ghost Fin metric which not only automatically tags the chips that are affected by Ghost Fin based, it gives us an idea of how bad the chip was affected by Ghost Fin.

SRAM

Fin Residue

* Does it look like a systematic or random defect?
  + Systematic
* How does it affect Pele yield at different voltage corners?
  + Not voltage dependent – hard fail
* Is the entire lot degraded or just a few wafers?
  + Not all wafers
* Does it affect both Pele 1 and Pele 2 in the same way?
  + Yes it does
* Is there any wafer regionality to the fails?
  + Bottom half of the wafer only
* Is there any slot level dependency?
  + Yes at FC RIE – either negative or positive
* Are there any splits on the lot?
  + No
* Look at the Cayce BFM to see what the fails look like. Are there patterns to the fail?
  + SCF or LoFBL at the bottom half of the wafer. Not dense.
* What kind of fails are occurring? BIT, DBC, DBR, etc
  + SCF, LoFBL
* Pull PattRec data for more detailed look
  + Stacked up all the fails and plotted by SRAM segment failing. Fails occurs on different segments on specific chips (hotspots) shows how systematic this issue is. Might be a tool problem
* Do a Pareto on PattRec data

Next I would look for correlations, do data mining, consult experts, while having regular updates to the rest of the team

* Ranked the wafers from worst to best based on my Fin Res Metric. Then pulled all the slot order data for each of the process steps. Found a slot order dependence occurring consistently at the FC RIE process step. One of the two tools was causing the issue.
* Stacked up all the fails and plotted by SRAM segment failing. Fails occurs on different segments on specific chips (hotspots) shows how systematic this issue is. Might be a tool problem
* Got TPLY to see the residue left around the Fins, causing a short from the Gate to TS

If it seems to be a recurring problem I would set up a form of monitoring the defect, write a classification algorithm to automatically label this issue and also come up with some sort of metric to label how much of an impact to yield this specific defect has.

* Made the Fin Res metric which helped track WIP, helped data mine (list of yes fin res vs no fin res), helped determine how much impact each wafer was hit with, finding tool signal, FQD5 tool hit way more often than FQD4, exclusion and triage

Root Cause:

Fin mandrel deposited -> spacer grows from it. RIE etching out the mandrel isn’t perfect, leaving behind residue. Gate and source drain contact is grown on top of the residue, causing shorts. Depending where it hits, we can get a bit fail or a LoFBL fail.

* If residual causes short between Gate and BL Contact, you can get a LoFBL
* If residual causes short between Gate and Ground Contact, you can get a SCF